Improved Memory Reliability against Multiple Cell Upsets: Survey

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Abstract – Scaling of CMOS technology to nanoscale will increase soft error rate in memory cells. Both single bit upset and Multiple Cell Upsets (MCUs) causes reliability issues in memory applications. Transient multiple cell upsets (MCUs) are getting major problems within the reliability of memories exposed to radiation environment and have an effect on large number of cells. Hence to provide fault tolerant memory cells, Error detection and Correction Codes are used which are being discussed here in this paper.

Index Terms – nanoscale, multiple cell upsets, soft error, reliability.

1. INTRODUCTION

When semiconductor devices are scaled right down to nanoscale, it causes threshold voltage variation, negative bias temperature instability, short channel, single bit upsets and multiple cell upsets. So to create memory cells fault tolerant Error Correction Codes (ECCs) are used. Most commonly used error correction codes are the hamming codes, bose Chaudhuri Hocquenghem codes and Reed solomon codes. Hamming code may be a set of error-correction code that's primarily used to detect and correct bit errors. It utilizes the idea of parity bits. Those parity bits are value-added to the information therefore as to make sure the validity of the data, while it's read or when it's been received during a data transmission. This error-correction code couldn't solely determine one bit error within the information unit, however additionally its location within the information unit by using over one parity bit. Once the quantity of ones is wrong, the parity count indicates that single bit errors are detected that successively reveals that an information bit has been flipped. Whereas using over one parity bit, hamming codes are capable of detecting 2 bit errors. The quantity of parity bits required depends on the quantity of bits that are sent during the information transmission. The main disadvantage of hamming code is that its capable of protecting only memories that are effected by single bit upsets. Bose Chaudhuri Hocquenghem codes are capable to correct a given range of bits in any position. Those codes use complicated or sophisticated decoding algorithms like complex algebraic decoders that decode in fixed time. Furthermore these are computationally very expensive. Reed Solomon groups the bits into blocks for correcting soft errors. The main disadvantage of those codes is that it needs complex decoding algorithms and tables of constants. All that error correction codes want a lot of space, power and delay overheads. Therefore interleaving technique is employed wherever the bits that belong to a similar logical word are placed apart such that MCU impact solely a little per word.

The impact of technology scaling has come to a level where reliability of memory gets affected. SRAM memory failure rates are increasing significantly, therefore posing a significant reliability concern in several applications. The sudden or unwanted changes within the value of a bit (or bits) within a memory is named as soft errors. Due to the sudden or random change in the data, it gets stored inside the memory as if it was a valid data. By means of replacement or restoring the erroneous data, the value of the system starts operating in the manner it should be. There are usually two types of soft errors, they are single bit upset and multiple cells upset. Single-bit upsets are errors that occur when only one bit of given information unit is modified from one to zero or from zero to 1. In multiple cell upset, 2 or a lot of bits within the information unit changes from zero to one or vice-versa. Such kind of errors doesn't mean that error happens in consecutive bits.

For detection and correction of errors, extra bits are added to every data byte of the memory. The extra bit that is added is called as parity check bit. Parity bits are the best type of error detecting codes. This parity bit is employed to determine whether or not the byte that's stored within the memory has the correct range of 0"s and 1"s in it. If the count changes, it indicates that there is an an error. There are two types of parity bits like even parity bit and odd parity bit. In the even parity bit, if the count of ones in the data is odd then the parity bit is set to one. If the count of ones is even then the parity bit is set to zero. In odd parity bit, if the count of ones in the given data is even then the parity bit is set to one. If the count of ones is odd then the parity bit is set to zero. But in some cases these parity bit itself may have an error and thus the error cannot be detected. For this purpose error correcting codes were used. An

algorithm that expresses a sequence of numbers, such that the errors that are present in it are often simply detected and corrected is named as an error-correction code. The study of error-correcting codes is called as coding theory. Error-correcting codes are much complex compared to error detecting codes moreover it requires much redundant bits. Due to this, the number of bits required to correct multiple bit errors are very high.

2. LITERATURE REVIEW

In [1] D. Radaelli, H. Puchner, S. Wong, and S. Daniel, has proposed the Multi-bit upset (MBU) events collected from accelerated soft error rate (SER) measurements performed with a quasi mono energetic neutron beam are studied with a threefold purpose. The first goal is to qualitatively access that if it is applicable and effective for the single-bit Error Detection and Correction algorithms and circuits (EDAC). The second goal is to see the connection with the memory core P-well tapping scheme. The third goal is to detect the "preferred" MBU shapes. The results reveal that the memory architecture is dangerous to affect the single-bit EDAC effectiveness. Also, tapping scheme is very important to reduce the MBU rate. Therefore finally it is analysed that the predominant MBU shape is strongly in influence with the vertical and horizontal distance of the active nodes of the memory cells. The results of this work show that the memory architecture is critical to affect the single-bit EDAC effectiveness. Particularly the bit-interleaving scheme that is implemented in the device under test protects physical MBU from being observed as data word MBUs. Physical MBUs are being detected as SBUs in different data words.

In [2] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, has discussed about the concepts in terrestrial neutron-induced soft-error in SRAMs from a 250 nm to a 22 nm process are being analyzed using the Monte-Carlo simulator CORIMS, which is predicted to have less than 20% variations in experimental soft-error data on 180–130 nm SRAMs in a large variety of neutron fields such as field tests at low and high altitudes and accelerator tests in LANSCE, TSL, and CYRIC. The following results are being obtained: 1) Soft-error rates per device in SRAMs is enhanced x6-7 from130 nm to 22 nm process; 2) As SRAM is being scaled down to a small size, soft-error rate is more by low-energy neutrons (<10 MeV); and 3) The area which is changed by one nuclear reaction passes over 1 M bits and bit multiplication of multi-cell upset has become as high as 100 bits and more.

In [3] C. Argyrides and D. K. Pradhan, has described a new decoding technique for triple error Reed-Muller codes. The Reed-Muller Codes (RMC) as on-chip triple error correcting scheme is discussed in this paper. The analysis of the area, delay and power overhead for incorporating RMC and widely used Hamming Codes into a register file is done. In this paper, a modified triple error RMC decoding circuit is presented. This technique can be used for highly memory architecture reliability. With the addition of ECC, the overall MTTF of the memory enhances to more than 440% when compared to the traditional Hamming codes. The graphical study reveals that there is a significant change in the reliability while on-chip error correcting code is added. It can be proved that with no error correcting codes the reliability drops in a great manner whereas the probability of error and memory size enhances. The ECC enhances the reliability and error tolerance. However it also improves the overall area and access time.

In [4] A. Sanchez-Macian, P. Reviriego, and J. A. Maestro has discussed that the radiation particle can influence registers or memories and create soft errors. These errors could change more than one bit causing a multiple cell upset (MCU) that contains errors in registers or memory cells which are physically related. These MCUs could influence a single word, creating adjacent bit errors. Hamming codes are generally used for shielding memories or registers from soft errors. Therefore, when multiple errors occur a Hamming code cannot detect them. In this paper, single-error-correction double adjacent error detection Hamming codes are discussed for 16-, 32-, and 64-bit words. Additionally, single-error-correction double-error-detection triple adjacent error detection codes based on extended Hamming are analyzed as well. The enhanced detection is obtained by doing a selective shortening and reordering of the Hamming matrix so the adjacent errors result in a syndrome that does not coincide to that of any single error. These codes will help in the detection of MCUs in SRAM memory designs.

In this paper, parity check matrices to implement SEC-DAED Hamming codes and SEC-DED-TAED in Hamming codes is presented. The results are obtained by selectively shortening the matrices so adjacent errors produce a syndrome that do not match any of those that match to a single error. The proposed scheme does not need any extra circuitry. The memory area, power and speed are the same as with the traditional bit placement. It can help in the detection of adjacent errors which are the ones that are due to Multiple Cell Upsets (MCUs) in SRAM memories.

In [5] S. Liu, P. Reviriego, and J. A. Maestro has discussed a single event upsets (SEUs) altering digital circuits that are getting a bigger problem for memory applications. This paper presents an error-detection method for difference-set cyclic codes with larger logic decoding. Many of the logic decidable codes are only suitable for memory applications because of their ability to correct a large number of errors. However, they require a large decoding time that influences memory performance. The proposed fault-detection method effectively decreases memory access time while there is no error in the data read. The technique uses the more logic decoder to detect failures, which makes the area overhead minimal and keeps the additional power consumption low.

In this paper, a fault-detection mechanism, MLDD, is presented based on ML decoding using the DSCCs. Exhaustive simulation test results show that the proposed technique will find pattern of up to 5 bit-flips within the initial 3 cycles of the decoding method. This improves the performance of the design with regard to the traditional MLD scheme. On the opposite hand, the MLDD error detector module is designed within the manner that's not dependent on the code size. This makes its area overhead much reduced when compared to other traditional approaches such as the syndrome calculation (SFD). In addition to this, a theoretical authority of the proposed MLDD scheme for the case of double errors is also presented. The extension of this proof to the case of four errors would make the validity of the MLDD approach for a more common case, something that has only been done through simulation in the paper. This is, therefore, an important problem for future research. The application of the proposed technique to memories which uses scrubbing is also an important topic and is in fact the original screw up which led to the MLDD scheme.

In [6] M. Zhu, L. Y. Xiao, L. L. Song, Y. J. Zhang, and H. W. Luo, has proposed a new MECC, which is called Mix code, to reduce MBUs in fault-secure memories. Considering the structural characteristic of MECC, euclidean geometry low density parity check (EG-LDPC) codes and hamming codes are joined within the proposed mix codes to preserve memories against MBUs with low redundancy overheads. Then, the fault-secure scheme is presented, that could manage transient faults in both the storage cell and the encoding and decoding circuits. The proposed fault-secure scheme has significantly lower redundancy overheads than the existing fault-secure schemes. Furthermore, the proposed scheme is opt for ordinary accessed data width (e.g., 2nbits) between system bus and memory. Finally, the proposed scheme has been executed in Verilog and validated through a large set of simulations. The experiment results show that the proposed scheme can efficiently reduce multiple errors in entire memory systems. They can not only mitigate the redundancy overheads of the storage array but also enhance the performance of MECC circuits in fault-secure memory systems.

This paper proposes a new fault-secure scheme to provide the reliability of memory in the presence of MBUs with low redundancy and performance overheads. The fault-secure scheme which is proposed can manage multiple errors in both the storage cells and the encoding and decoding circuits. Its redundancy bits are significantly lesser than the existing fault-secure scheme. The proposed fault-secure scheme suits in all ordinary bit width in memories. In order to get the above characteristics a new codeword structure, which is called a Mix code is shown. The proposed Mix codes use the layout architecture of codeword and combine EG-LDPC codes with Hamming codes to correct MBUs in memories. When protecting the same width data bits, the Mix codes have remarkably lower redundancy overheads when compared with that of EG-LDPC codes. The correction capability of Mix codes is equal to that of combined EG-LDPC code. In addition, Mix codes can save some data that EG-LDPC codes cannot manage with. Some conclusions can be taken from this paper. At First, by using the proposed fault-secure scheme, at least two errors can be corrected in the entire memory system (i.e., storage array, encoder, decoder and detector). If the correction ability of memory needs to be enhanced, the more powerful MECC can be added in the proposed scheme. Secondly, when the correction capability of the proposed fault-secure scheme is more than two bits, the correction ability of combinational circuits cannot reach 100%. But it can keep high level and is very close to 100%. Thirdly, different failure probabilities of the storage array and combinational circuits influence the MTTF of a memory system. Fourthly, the code rate of the proposed fault-secure scheme is greater than that of EG-LDPC codes, which causes lesser redundancy bits. The correction efficiency of the proposed scheme is nearer to that of EG-LDPC code scheme.

In [7] R. Naseer and J. Draper has described the range of SRAM multi-bit upsets (MBU) in sub100nm technologies is characterized using irradiation tests on two prototype ICs, developed in 90nm commercial processes. Results indicate that MBU as large as 13-bit could happen in these technologies limiting the efficiency of the conventional SEC-DED error-correcting codes (ECC). A double-error correcting (DEC) ECC implementation technique opt for SRAM applications is presented. Results show that this DEC scheme mitigates errors by 98.5% compared to only 44% reduction by conventional SEC-DED ECC.

Heavy-ion-induced soft error results in SRAM ICs designed in two characteristic 90nm processes have been presented. The upset distributions reveals that MBUs are the great contributor to overall soft error rate, and those MBU can be ranged as large as 9-bits for LP and 13-bits for SF for the usage of more powerful ECC schemes. Implementations of DEC and DEC-TED ECC using a parallel implementation approach in 90nm technology shows that these codes can effectively be implemented for SRAM applications. Synthesis outputs for different ECC circuits reveal various trade-offs and gives guidance for choosing a particular solution that depends on the application requirements. Test conclusions on prototype SRAM ICs demonstrate that DEC mitigates the error count by more than 98% when compared to only 44% for SEC-DED ECC.

In [8] G. Neuberger, D. L. Kastensmidt, and R. Reis, has described that Modern SoC architectures designed at decreasing geometries use multiple embedded memories. Error detection and correction codes have become more important for enhancing the fault tolerance of embedded memories. This paper is based on automatically reducing classical Reed-Solomon codes by selecting the opt code polynomial and set of

used symbols. The RS-OPGE tool permits for more accurate comparisons between previously manually implemented cores and more complex reduced cores, this capability allows us to analyze the proposed techniques' efficiency. The smallest logic units are revealed in the FPGA. The FPGA characterizes four LUTs combined with two flip-flops and a set of small glue logic as two slices is shown in one configurable logic block (CLB). The performance estimation is obtained from the timing report. The delay is related to the number of slices (LUTs) in cascade and the routing.

3. CONCLUSION

The above discussed papers fail to assure the reliability of memory, more number of errors were not detected and corrected and does not provide protection level against large MCUs in memory and finally requires more redundant bits and hence therefore as a future work a new technique which solves the above problems can be done.

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